2 MJ 60504

FOUR YEAR (Honours) B.Sc. (CBCS) DEGREE EXAMINATION, APRIL/MAY 2024

SECOND SEMESTER

Computer Science

Course IV : DIGITAL LOGIC DESIGN – MAJOR

(*w.e.f. 2023–24 Admitted Batch*)

Time : Three hours

Maximum : 70 marks

(No additional sheet will be supplied)

SECTION A — (5 × 4 = 20 marks)

Answer any FIVE of the following questions.

Each question carries equal marks.

1. Explain 2's complement method for subtraction.
2. Explain about signed binary number with examples.
3. Explain about NOT, AND, OR gates with truth tables.
4. Design X – OR and X – NOR gates using universal gates.
5. Draw the block diagram of full-subtractor with truth table.
6. Explain the difference between combinational and sequential circuits.
7. Explain the distinguish between Multiplexer and Demultiplexer.
8. Write a short note on classification of sequential circuits.
9. Explain the operation of RS flip flop.
10. Explain the POS and SOP logic functions.

SECTION B — (5 × 10 = 50 marks)

Answer FIVE of the following questions.

Each question carries equal marks.

11. Discuss in detail about Binary, Decimal, Hexadecimal and Octal number systems with examples.

Or

12. Add and subtract in binary

    (a) 110110 and 11101 (b) 100100 and 10110 (c) 1101001 and 11011

13. What is K-map? Explain how it help in simplifying a given Boolean expression. Draw k-map for four variables.

Or

14. NAND and NOR gates called as universal gates. Explain.

15. Design full adder and half subtractor by using universal Gates.

Or

16. Explain half adder with truth table. Implement the fill adder using two half adder.

17. Explain the working of Demultiplexer and Decoder circuit diagram.

Or

18. Explain the working of 8 line to 3 line encoder with truth table.

19. What is difference between latch and flip-flop? Explain about clocked RS flip flop using NAND gate.

Or

20. Convert D flip flop into RS flip flop and JK flip flop.
